Amendments to the Specification:

The following title will replace all previous titles identified with this application:

NONVOLATILE SEMICONDUCTOR DEVICE WITH FLOATING GATE STRUCTURE

Please replace the paragraph beginning at page 2, line 4, with the following rewritten paragraph:

Taking account of these requirements for such a cell array and its peripheral circuit, for conventional ~~flush~~ flash memory, the following manufacturing process is used. Figs. ~~Fig.~~ 35(a) through 35(d) show major steps noticing the cell array region. As shown in Fig. 35(a), a silicon substrate 1, having formed a tunnel oxide layer 2 thereon and a polycrystalline silicon film 3a on the tunnel oxide layer 2, is separated into respective device regions by STI (shallow trench isolation) technology. That is, device isolation grooves 4 are made by RIE, and they are buried with a device isolation insulation film 5 as shown in Fig. 35. The polycrystalline silicon film 3a will serve as a base layer of floating gates.

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Please replace the paragraph beginning at page 4, line 7, with the following rewritten paragraph:

In the conventional process reviewed above, in the peripheral circuit region ~~needs removing~~ the tunnel oxide film formed over both the peripheral circuit region and the cell array region needs to be removed, newly forming a gate oxide film for high-voltage circuit transistors, then ~~selectively removing~~ the gate oxide film is selectively removed by etching and thereafter ~~forming~~ a gate oxide film is formed for low-voltage circuit transistors. Repeating such etching steps of oxide films several times causes, in the peripheral circuit

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region, retraction of the device isolation insulating film already buried. Fig. 36(a) shows an aspect of such retraction. If the gate oxide film 8 is formed as shown in Fig. 36(b) on the structure shown in Fig. 36(a) to make gate electrodes 9, edge portions of the gate electrodes 9 enter into the concave portions of the device isolation insulating film in contact with side surfaces of device regions as shown by the broken line A.

Please replace the paragraph beginning at page 6, line 2, with the following rewritten paragraph:

selectively etching the second-layer gate electrode material film to separate the same on the device isolating insulating film in the cell array region;

Please replace the paragraph beginning at page 10, line 22, with the following rewritten paragraph:

The present invention ensures impurity doping individually optimum for floating gates and control gates of memory cells, and gate electrodes of the peripheral circuit. In addition, ~~At~~ at least the bottom layer of gate electrodes in the cell array region and the peripheral circuit region is stacked before the device isolation insulating film is buried, and remains in self-alignment with the device isolation insulating film. Therefore, unlike the process of making gate insulating films different in thickness through a plurality of etching steps of oxide films after burying the device isolation insulating film, here is prevented retraction of the device isolation insulating film in the peripheral circuit region, and property and reliability of the peripheral circuit transistors can be improved.

Please replace the paragraph beginning at page 11, line 7, with the following rewritten paragraph:

Fig. 3 is a cross-sectional view that shows a step of selectively removing a gate insulating film of a ~~lo-voltage~~ low-voltage circuit in the first embodiment;

Please replace the paragraph beginning at page 12, line 10, with the following rewritten paragraph:

Fig. 16 is a cross-sectional view that shows a step of forming a block film in the ~~second embodiment~~;

Please replace the paragraph beginning at page 14, line 20, with the following rewritten paragraph:

Subsequently, as shown in Fig. 3, the cell array region and the high-voltage circuit region in the peripheral circuit region are covered with a resist 23, for example, and the gate ~~insulting~~ insulating film 21b is selectively removed by etching from a low-voltage circuit region in the peripheral circuit region. Thereafter, thermal oxidation is conducted to form a gate oxide film 21c required in the low-voltage circuit region as shown in Fig. 4. For example, if the gate oxide film 21b of the high-voltage circuit requires the thickness of 17 nm, it is initially made to be approximately 14 nm thick. If the gate oxide film 21c of the low-voltage circuit is formed to a thickness around 8 nm, during this oxidation process, thickness of the gate oxide film 21b of the high-voltage circuit is increased to about 17 nm.

Please replace the paragraph beginning at page 23, line 7, with the following rewritten paragraph:

In addition, the instant embodiment does not use ion implantation upon introducing phosphorus into the floating gates of memory cells. That is, phosphorus is doped into the second-layer polycrystalline silicon film when stacking it, and it is diffused by solid-phase diffusion into the first-layer polycrystalline silicon film forming the bottom layer of the floating gates. Therefore, damage to the tunnel oxide film and other adverse ~~affection~~ affects by channeling are prevented unlike the process relying on high-concentrated phosphorus ion implantation.

Please replace the paragraph beginning at page 24, line 36, with the following rewritten paragraph:

After that, upper part of the second-layer polycrystalline silicon film 24 containing phosphorus is removed by CMP. As a result, as shown in Fig. ~~13~~ 30, in the cell array region, the second-layer polycrystalline silicon film 24 is maintained in a self-aligned manner solely in the memory cell regions interposed between separate adjacent regions of the device isolation insulating film 14 and used together with the first-layer polycrystalline silicon film 22 to form floating gates. After that, as shown in Fig. 31~~C~~, while covering the cell array region with a resist 61, the second-layer polycrystalline silicon film 24 still remaining the peripheral circuit region is removed by CDE(Chemical Dry Etching).